

N and P Channel 30V MOSFET

General Description

The JY12M is the N and P Channel logic enhancement mode power field transistors are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

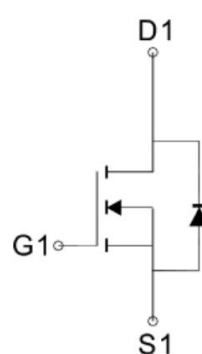
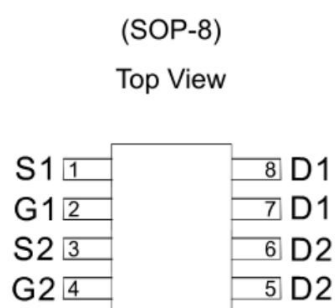
Device	R _{DS(ON)} MAX	I _D MAX(25° C)
N-Channel	20mΩ@V _{GS} =10V	8.5A
	32mΩ@V _{GS} =4.5V	7.0A
P-Channel	45mΩ@V _{GS} =-10V	-5.5A
	85mΩ@V _{GS} =-4.5V	-4.1A

- Low Input Capacitance
- Fast Switching Speed

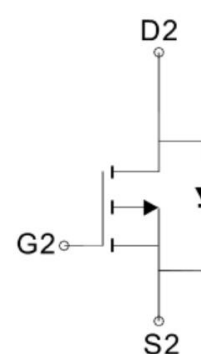
APPLICATIONS

- Power Management
- DC/DC Converter
- DC Motor Control
- LCD TV & Monitor Display Inverter
- CCFL inverter

PIN DESCRIPTION



N-Channel MOSFET



P-Channel MOSFET

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Absolute Maximum Ratings(Ta=25°C Unless Otherwise Noted)

Parameter		Symbol	N Channel		P Channel		Unit
			10 sec	Steady	10 sec	Steady	
Drain Source Voltage		V _{DSS}	30		-30		V
Gate Source Voltage		V _{DSS}	± 20		± 20		
Continuous Drain Current	Ta=25 °C	I _D	8.5	6.5	-7.0	-5.3	A
	Ta=70 °C		6.8	5.1	-5.5	-4.1	
Pulsed Drain Current		I _{DM}	30		30		
Maximum Power Dissipation	Ta=25 °C	P _D	1.5				W
	Ta=70 °C		0.95				
Operating Junction Temperature		T _J	-55 to 150				°C
Thermal Resistance Junction to Ambient		R _{θJA}	61	100	62	103	°C/W
Thermal Resistance Junction to Case		R _{θJC}	15		15		°C/W

Electrical Characteristics(Ta=25°C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Static							
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250uA	N-Ch	1.0	1.5	3.0	V
		V _{DS} =V _{GS} ,I _D =-250uA	P-Ch	-1.0	-1.5	-3.0	
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V	N-Ch			±100	nA
			P-Ch			±100	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V	N-Ch			1	uA
		V _{DS} =-30V, V _{GS} =0V	P-Ch			-1	
I _{D(ON)}	On-State Drain Current	V _{DS} ≥5V, V _{GS} =10V	N-Ch	20			A
		V _{DS} ≤-5V, V _{GS} =-10V	P-Ch	-20			
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V,I _D =7.4A	N-Ch		15	20	mΩ
		V _{GS} =-10V,I _D =-5.2A	P-Ch		38	45	
		V _{GS} =4.5V,I _D =6.0A	N-Ch		23	32	
		V _{GS} =-4.5V,I _D =-4.0A	P-Ch		65	85	
V _{SD}	Diode Forward Voltage	I _S =1.7A,V _{GS} =0V	N-Ch		0.8	1.2	V
		I _S =-1.7A,V _{GS} =0V	P-Ch		-0.8	-1.2	

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Electrical Characteristics(Ta=25°C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic						
Qg	Total Gate Charge	N-Channel V _{DS} =15V, V _{GS} =10V, I _D =10A	N-Ch		9.8	nC
			P-Ch		10.5	
Qgs	Gate-Source Charge	P-Channel V _{DS} =-15V, V _{GS} = -10V, I _D =-6A	N-Ch		1.6	
			P-Ch		1.8	
Qgd	Gate-Drain Charge		N-Ch		2.0	
			P-Ch		1.9	
Ciss	Input Capacitance	N-Channel V _{DS} =15V, V _{GS} =0V, f=1MHz	N-Ch		501	pF
			P-Ch		590	
Coss	Output Capacitance	P-Channel V _{DS} =-25V, V _{GS} =0V, f=1MHz	N-Ch		72	
			P-Ch		69	
Crss	Reverse Transfer Capacitance		N-Ch		57	
			P-Ch		53	
Rg	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	N-Ch		1.84	Ω
			P-Ch		11	
T _{d(on)}	Turn-On Delay Time	N-Channel V _{DD} =15V, V _{GS} =10V, R _G =6Ω, I _D =1A	N-Ch		3.9	ns
			P-Ch		6.8	
T _r	Turn-On Rise Time	P-Channel V _{DD} =-15V, V _{GS} =-10 V, R _G =6Ω, I _D =-1A	N-Ch		4.2	
			P-Ch		4.9	
T _{d(off)}	Turn-Off Delay Time		N-Ch		16.6	
			P-Ch		284	
T _f	Turn-Off Fall Time		N-Ch		5.5	
			P-Ch		12.4	
T _{rr}	Reverse Recovery Time	I _F =12A, di/dt=500A/us	N-Ch		5.5	ns
			P-Ch		14	
Q _{rr}	Reverse Recovery Charge		N-Ch		2.6	nC
			P-Ch		11	

*The device mounted on 1in2 FR4 board with 2oz copper.

*Guaranteed by design. Not subject to product testing.

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Typical Characteristics(T_J=25°C Noted)

N-Channel

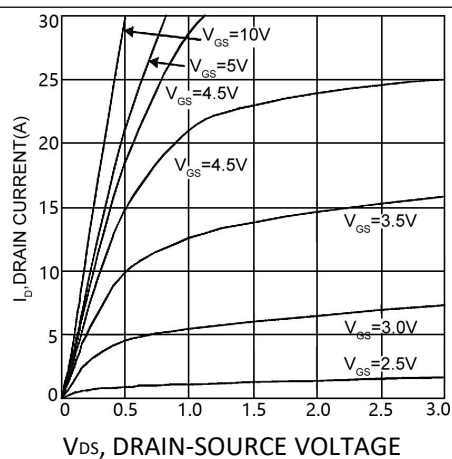


Figure1. Typical Output Characteristic

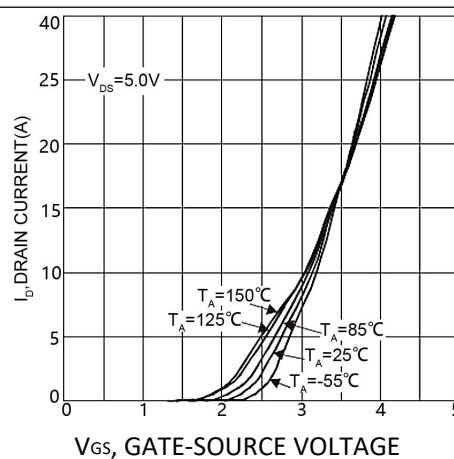
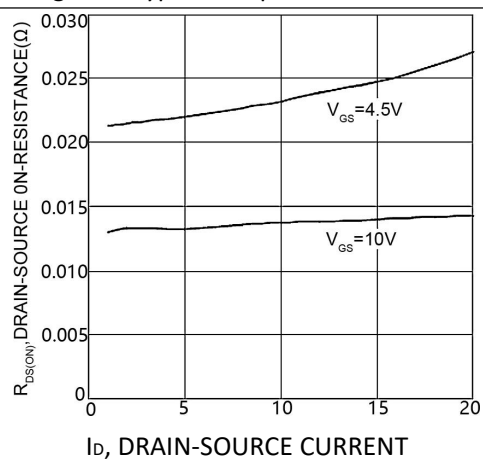
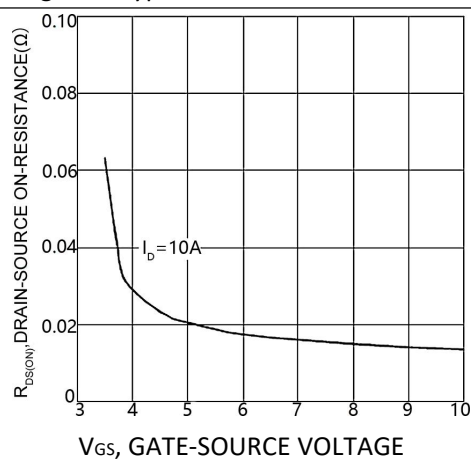
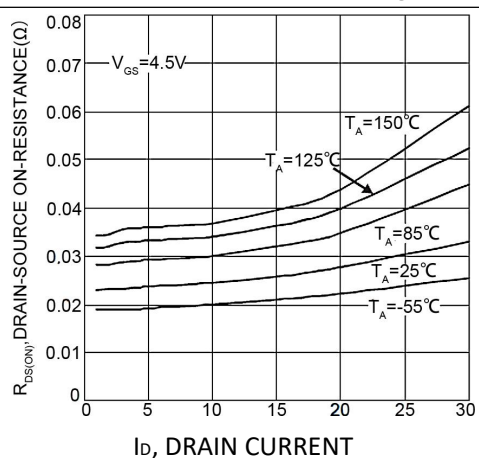
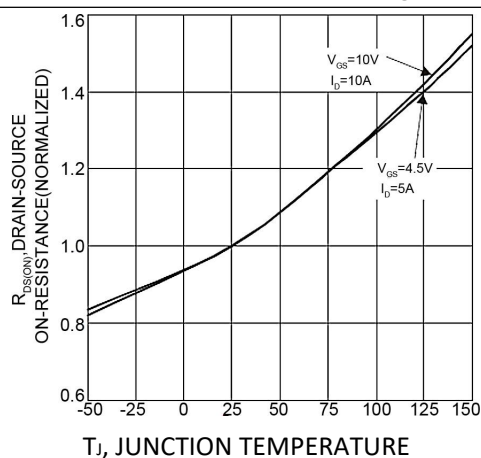


Figure2. Typical Transfer Characteristic

Figure3. Typical On-Resistance vs.
Drain Current and Gate VoltageFigure4. Typical On-Resistance vs.
Drain Current and Gate VoltageFigure5. Typical On-Resistance vs.
Drain Current and TemperatureFigure6. On-Resistance Variation with
Temperature

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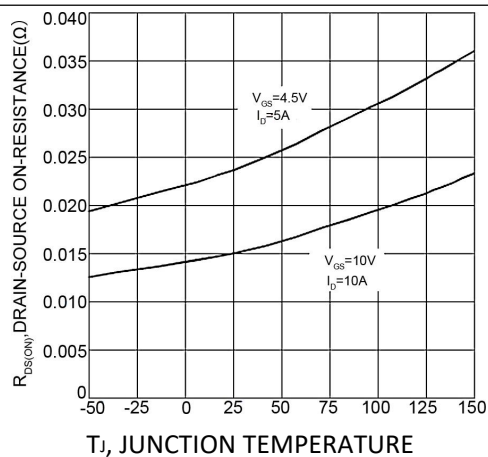
Typical Characteristics(T_J=25°C Noted) N-Channel

Figure7.On

-Resistance Variation with Temperature

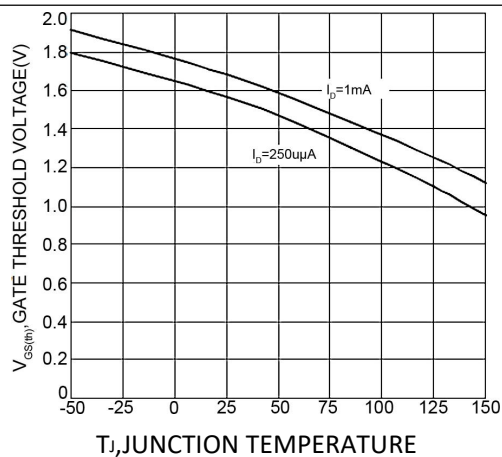


Figure8. Gate Threshold vs. Ambient Temperature

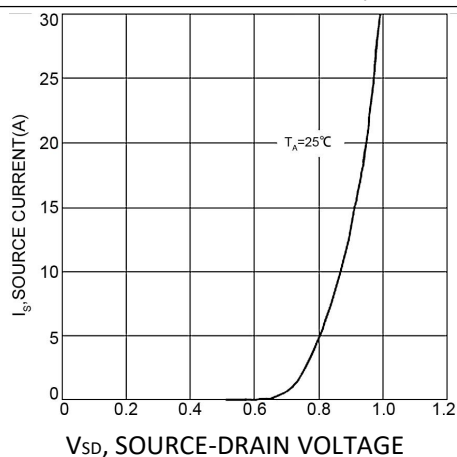


Figure9.Diode Forward Voltage vs. Current

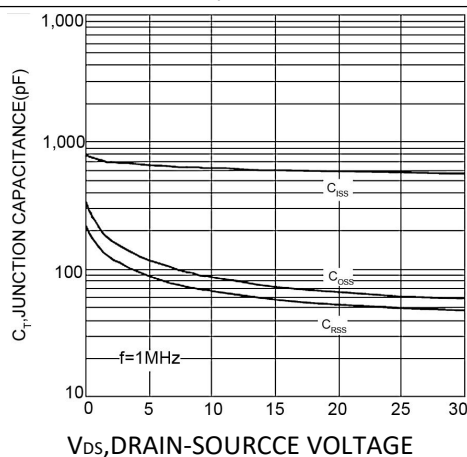


Figure10. Typical Junction Capacitance

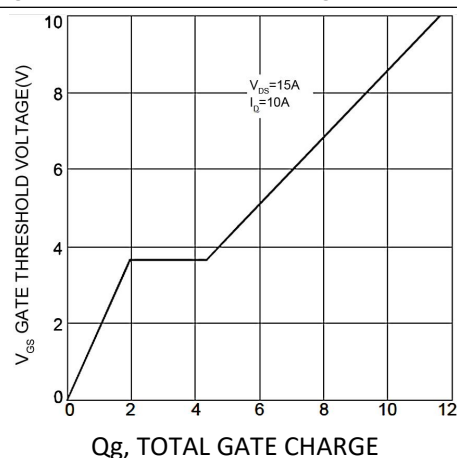


Figure11. Gate Charge

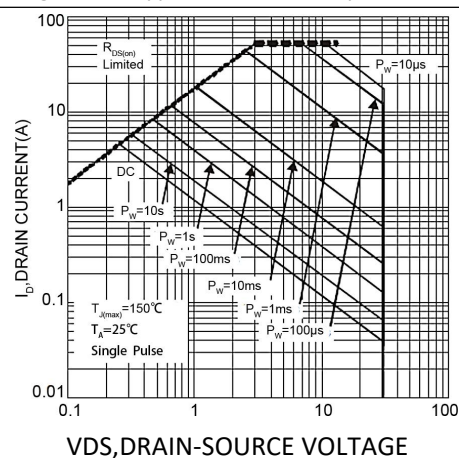


Figure12. SOA, Safe Operation Area

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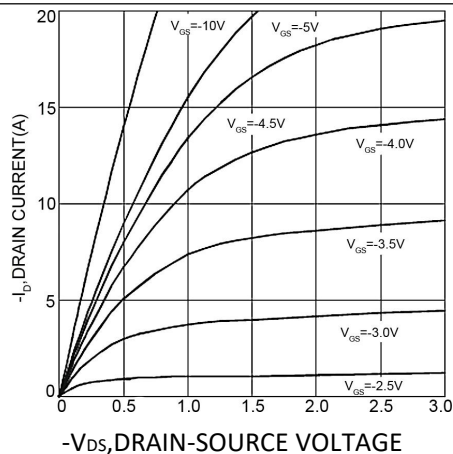
Typical Characteristics($T_J=25^\circ\text{C}$ Noted) P-Channe

Figure13. Typical Output Characteristics

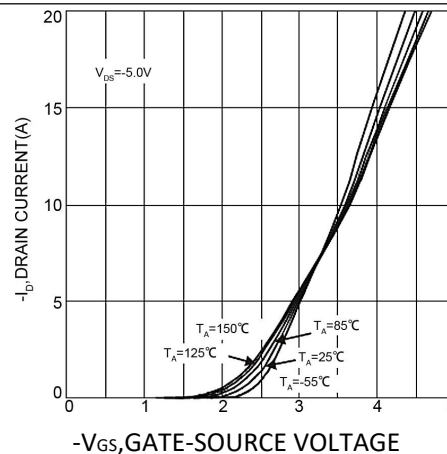
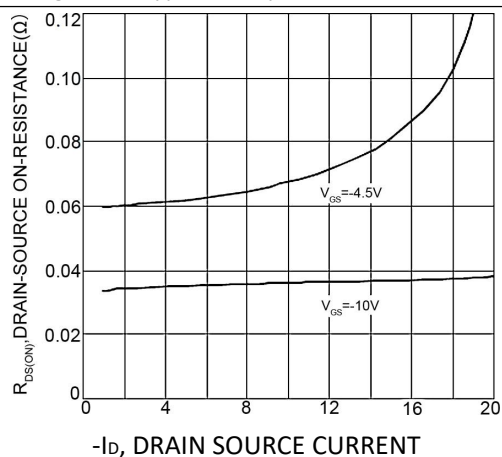
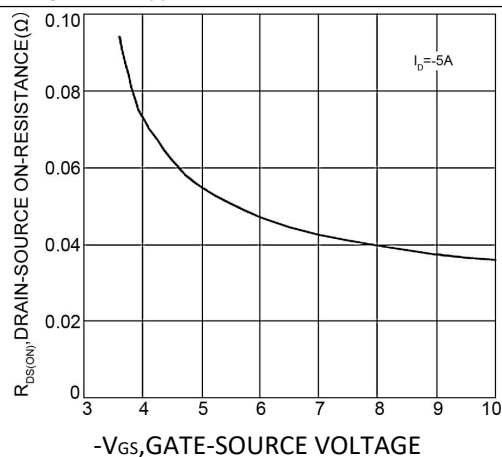
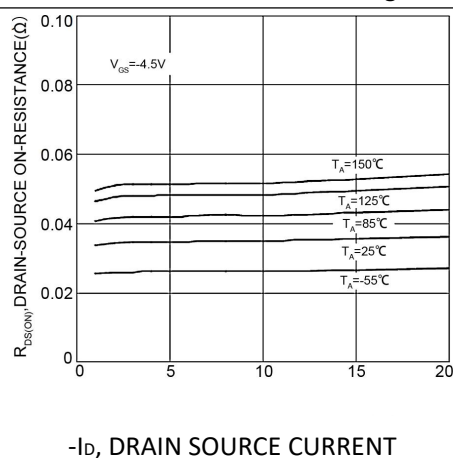
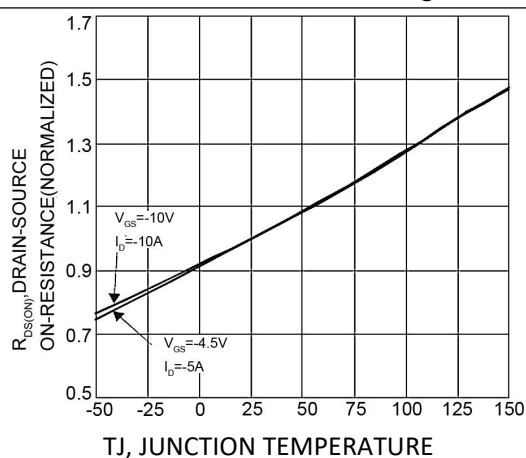


Figure14. Typical Transfer Characteristics

Figure15. Typical On-Resistance vs.
Drain Current and Gate VoltageFigure16. Typical On-Resistance vs.
Drain Current and Gate VoltageFigure17. Typical
On-Resistance vs.
Drain Current and TemperatureFigure18. On
-Resistance Variation with
Temperature

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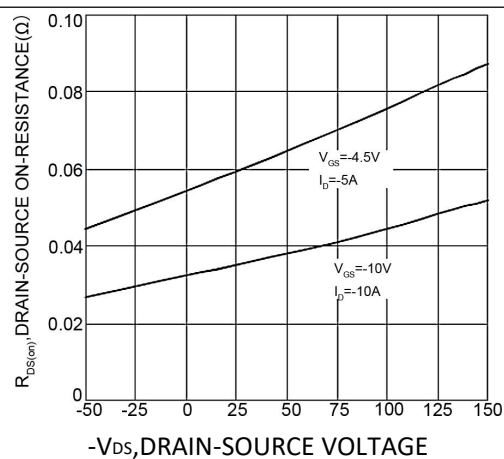
Typical Characteristics(T_J=25°C Noted) P-Channel

Figure19. On-Resistance Variation with Temperature

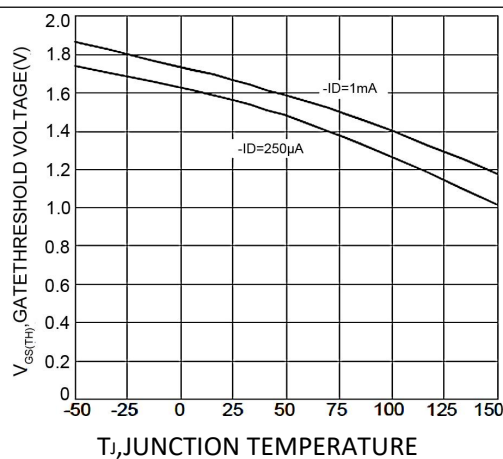


Figure20. Gate Threshold vs. Ambient Temperature

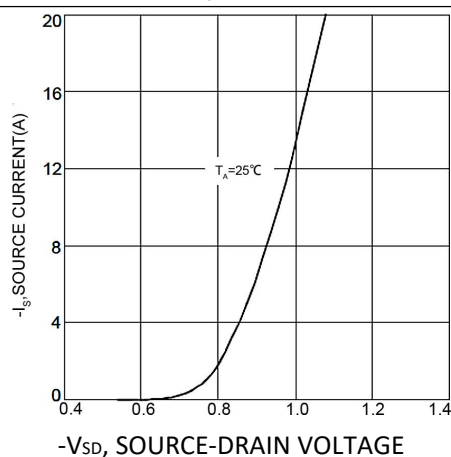


Figure21. Diode Forward Voltage vs. Current

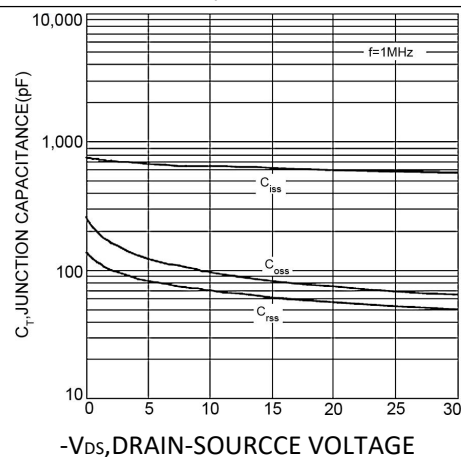


Figure22. Typical Junction Capacitance

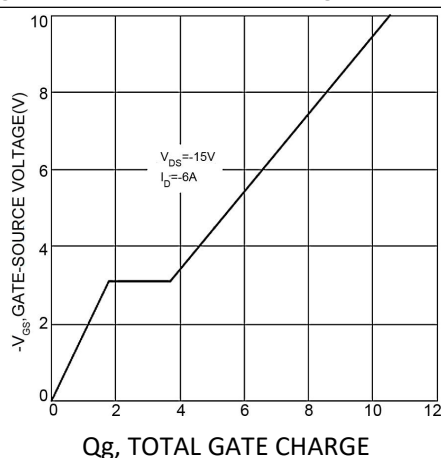


Figure23. Gate Charge

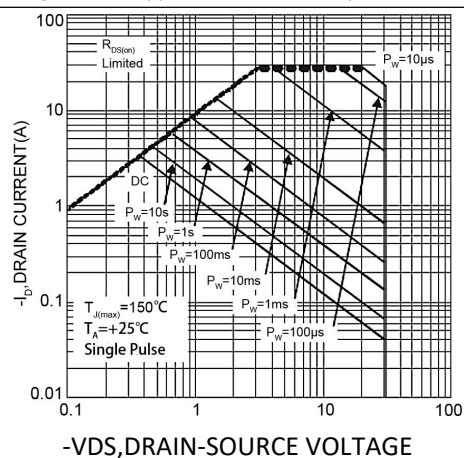


Figure24. SOA, Safe Operation Area

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SOP-8 Package Outline

